Modeling and Simulation of Poly-crystalline Silicon Thin Film Transistor for Improved Gate Transport Efficiency

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Abstract — In this work, a two-dimensional potential distribution formulation/model is presented for modified Schottky gate contact poly-crystalline silicon thin film transistors. The work aims at deriving potential solution and in this way trying to limit the impact of punch-through condition. Green’s function approach is adopted for the two-dimensional potential solution. The developed formulation incorporates the effects due to traps, grain-boundaries, short-channel and drain-induced barrier lowering (DIBL). The results obtained show good agreement with simulation results, thus demonstrating the validity of our model.

Index Terms— Device modeling, poly-Si TFT, grain-boundary effect.

I. INTRODUCTION

As a result of application of high speed pixel switching devices in active matrix liquid crystal displays (AMLCDs) [1], poly-crystalline silicon (poly-Si) thin film transistors (TFTs) are receiving significant attention. Poly-Si TFTs are also used as drivers in high-resolution active-matrix microencapsulated electrophoretic display (EDP) [2]. The miniaturization of poly-Si TFTs is being actively pursued in order to improve the aperture ratio and ensuring high performance of devices [3-4]. But as the physical dimensions reduce, higher electric fields are generated which leads to hot electron injection into the gate. The hot electron injection can be minimized using drain engineered structures as in MOSFETs [5]. Such structures lead to a decrease in peak electric field near drain but shift its position near to the drain end. A structure is required which not only reduces electric field near the drain but keeps the peak of electric field under the gate ensuring more control of gate over the conductance of channel. In this structure gate Schottky contact is modified and comprises of two metals with different work-functions but zero spacing defined as dual-material gate (DMG) and will serve the purpose. This structure has inherent advantage of improving the gate transport efficiency by modifying the electric field pattern and surface potential along the channel.

This article focuses on the variation of potential distribution along the device with modified Schottky gate contact. The potential pattern is modeled by solving two-dimensional (2-D) Poisson’s equation. The scheme adopted to solve Poisson’s equation is Green’s function. The effect of change in device length, gate-bias, drain-bias, gate work-function etc. is studied. The modeled results are found to be in good agreement with simulated results.

II. MODELING AND DISCUSSION

The schematic view of the structure can be seen in Fig.1 and comprises of poly-silicon film sandwiched between gate and buried oxide. The point \( x_{pl} \) represents the joining position of two different work-function gate electrodes. The break line resembles any number of grains present in the poly-Si film; \( L \) is the channel...
length, \( L_g \) is grain-size, \( L_{gb} \) is the grain-boundary, \( t_{ox}^g \), \( t_{poly} \) and \( t_{ox}^b \) represents the gate-oxide thickness, thickness of poly-Si film and buried-oxide thickness respectively.

A. Formulation

The potential distribution model for the poly-Si TFT is obtained by solving two-dimensional Poisson’s equation given as:

\[
\left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) \Phi(x, y) = -\frac{\rho(x, y)}{\varepsilon} \quad(1)
\]

where \( \Phi(x, y) \) is the 2-D potential distribution, \( \varepsilon = \varepsilon_0(\varepsilon_{Si}) \) is dielectric permittivity of \( Si(SiO_2) \) and \( \rho(x, y) \) is the 2-D space charge density in the different sections.

\[\text{Table 1: Space charge density for poly-Si TFT with two material gates}\]

<table>
<thead>
<tr>
<th>( -t_{ox}^g \leq y \leq 0 )</th>
<th>( 0 \leq y \leq t_{poly} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>if ( Y_d(x) \geq t_{poly} )</td>
<td>( N_g )</td>
</tr>
<tr>
<td>( N_{gb} )</td>
<td>( 0 \leq y \leq t_{poly} ) for GR</td>
</tr>
</tbody>
</table>

\[\rho(x, y) = \begin{cases} 
0 & \text{for} \quad 0 \leq y \leq t_{poly} \\
N_{g} & \text{if} \quad Y_d(x) \geq t_{poly} \\
N_{gb} & \text{if} \quad 0 \leq y \leq t_{poly} \quad \text{for GB} \\
0 & \text{if} \quad Y_d(x) < t_{poly} \quad \text{for GR} \\
0 & \text{if} \quad Y_d(x) \leq y \leq t_{poly} \quad \text{for GB} \\
0 & \text{if} \quad t_{poly} \leq y \leq t_{poly} + t_{ox}^b \\
\end{cases} \]

where GR(GB) represents grain(grain-boundary) region, \( N_{gb} \) is the doping concentration in grain(grain-boundary) and incorporates effects due to traps [6-7]. \( Y_d(x) \) is the one-dimensional depletion width.

The formulation for poly-silicon film i.e. the section of concern is given as:

\[\Phi_{Si}(x, y) = \int \frac{\rho(x', y')}{\varepsilon} G(x, y; x', y')dx' dy' + C_{DO}^H \left( 1 - \frac{x}{L} \right) + C_{DO}^V \left( \frac{x}{L} \right) + \sum_{m=1}^{\infty} \left( \frac{\cos(k_m y)}{\sinh(k_m L)} \left( C_s^H \sinh(k_m (L - x)) + C_s^H \sin(k_m x) \right) \right) \sin(k_m x) \left( D_s^b \cosh(k_m (t_{poly} - y)) - D_s^b \cosh(k_m y) \right) + \sum_{m=1}^{\infty} \frac{D_{Si}^b \sinh(k_m t_{poly})}{k_m \sinh(k_m t_{poly})} \quad(3)\]

where \( G(x, y; x', y') \) is Green’s function, \( V_{bi} \) is the built-in potential of the source(drain)/ body junctions and \( V_{di} \) is drain-source voltage. \( V_{sep}(x) = V_{gr} - V_{gr}'(x) \) in which \( V_{gr} \) is gate-source...
voltage and \( V_g^f(x) \) is the modified flat-band voltage for the gate oxide. \( k_g^l = (n-0.5) \cdot \pi / t_{ox}^l \), \( k_g^u = n \cdot \pi / t_{poly} \) and \( k_u^m = (n-0.5) \cdot \pi / t_{ox}^u \) defines the eigenvalue along \( y \) direction for different sections and \( k_m = m \cdot \pi / L \) is the eigenvalue in all sections along \( x \) direction. \( \phi_0^j \left( C_{poly} \right) \). \( \phi_0^j \left( C_{poly} \right) \) and \( D_m^b \) are the Fourier coefficients of the potential at source(drain) for \( n=0, n=n \) and electric field displacement at the \( Si-SiO_2 \) interface at gate side (buried oxide side) respectively (see APPENDIX).

Table 2: The List of Boundary Conditions used in the analysis for different sections

<table>
<thead>
<tr>
<th>Section</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>( \phi^I(x-y_{ox}^I) = V_{eff}^I(x) = V_{gs} - V_g^f(x) )</td>
</tr>
<tr>
<td></td>
<td>( \phi_0(0,y) = V_{bi} + \frac{V_{bi} - V_{eff}^I(0)}{y} )</td>
</tr>
<tr>
<td></td>
<td>( \phi^I(L,y) = V_{bi} + \frac{V_{bi} + V_{ds} - V_{eff}^I(L)}{y} )</td>
</tr>
<tr>
<td></td>
<td>( D^I(x,0) = \varepsilon_{ox} E_{y}^I(x,0) )</td>
</tr>
<tr>
<td></td>
<td>( D^I(x,y) = \varepsilon_{ox} E_{y}^I(x,y) )</td>
</tr>
<tr>
<td>II</td>
<td>( \phi^{II}(0,y) = V_{bi} )</td>
</tr>
<tr>
<td></td>
<td>( \phi^{II}(L,y) = V_{bi} + V_{ds} )</td>
</tr>
<tr>
<td></td>
<td>( D^I(x,t_{poly}) = \varepsilon_{ox} E_{y}^I(x,t_{poly}) )</td>
</tr>
<tr>
<td></td>
<td>( D^I(x,0) = \varepsilon_{ox} E_{y}^I(x,0) )</td>
</tr>
<tr>
<td></td>
<td>( \phi_{0}^{II}(0,y) = V_{bi} )</td>
</tr>
<tr>
<td></td>
<td>( \phi_{0}^{II}(L,y) = V_{bi} + V_{ds} - \frac{V_{bi} + V_{ds}}{t_{ox}^b} )</td>
</tr>
<tr>
<td></td>
<td>( \phi_{0}^{II}(x,t_{poly} + t_{ox}^b) = 0 )</td>
</tr>
</tbody>
</table>

The derived formulation for potential is used to determine distribution along the channel of the poly Si TFT. The comparison of modified gate Schottky contact with single-material gate structure is carried out in this analysis. The solution obtained is derived assuming the boundary conditions listed in Table 2.

![Fig.2. Variation of surface channel potential with normalized channel distance for different ratio of metal gates and different drain-source voltages.](image)

The variation of surface channel potential with normalized channel distance with simulated results [10] is plotted in Fig.2 for device dimensions of \( L=0.6 \mu m \), \( t_{ox}^l = 45nm \), \( t_{poly} = 40nm \) and \( t_{ox}^b = 45nm \). The figure shows the impact of variation in the joining position of two different work-function gate electrodes at different drain-source voltages. It is seen from the figure that use of modified Schottky contact limits the impact of drain end depletion over the channel. The effects due to traps and grain-boundaries are realized as a kink at the grain-boundary. Also we can see the shift in minima position along the channel length as we increase the drain-source voltage. Thus the figure shows the incorporation of short channel effects and drain-induced barrier lowering. The modeled results are in good agreement with the simulated results and prove validity of the formulation.

Fig.3 shows the channel potential variation with normalized channel distance for single-material gate and double-material gate at different device dimensions and \( x_{pl} = 0.2 \mu m \). The results obtained matches well with simulated results.
The idea behind tracing the curves computed from the model for different device dimensions is to prove the versatility of our model. The use of modified Schottky contact seems to be a better choice than adopting LDD [11-12] or GOLDD [13] structures as the introduction of additional doping increases the device resistances whereas modified Schottky contact serve as an external device parameter.

Fig.3. Variation of surface channel potential with normalized channel distance for different channel lengths (SMG=single-material gate, DMG=dual-material gate).

The surface channel potential variation with normalized channel distance in Fig.4 is drawn to show the consequence of setting the two different gate work-functions. The modeled results satisfy the simulated results [10] remarkably. It is seen from the figure that as the metal work-function towards drain-end increases with source-end assumed to be constant value; the shift in the minima value and position is seen. This shows that although the introduction of metal work-function limits the drain depletion to overlap the channel depletion, but it needs to be optimized as an excess gap in values of metal work-function will not solve the purpose. Also the analysis for source-end keeping drain end metal work-function to be constant is done. The curves show the shift of minima position towards the drain end. Thus one can realize this asymmetric structure as symmetric for optimized value of drain-source voltage. In this way this idea gives room to utilize increased value of drain-source voltage with minimal effect over the channel as it reduces the peak of electric field at the drain-end.

Fig.4. Variation of surface channel potential with normalized channel distance for different metal work-functions along source end and drain end.

III. CONCLUSION

A 2-D potential distribution formulation/ model is presented for modified Schottky gate contact poly-crystalline silicon thin film transistors adopting Green’s function approach. The developed formulation incorporates the effects due to traps, grain-boundaries, short-channel effects and drain induced barrier lowering (DIBL) effects and can be seen from the characteristics. A comparison of SMG TFT with DMG TFT characteristics is analyzed and enhancement of device performance is seen on application of modified Schottky gate contact. The results obtained show good agreement with
simulation results, thus demonstrating the validity of our model.

**APPENDIX**

\[ C_{s_0}^i = \frac{1}{(\alpha_2 - \alpha_1)} \int_{a_i}^{a_2} \phi'(0, y') dy' \]  
\[ (A1) \]

\[ C_{d_0}^i = \frac{1}{(\alpha_2 - \alpha_1)} \int_{a_i}^{a_2} \phi'(L, y') dy' \]  
\[ (A2) \]

\[ C_s^i = \frac{2}{(\alpha_2 - \alpha_1)} \int_{a_i}^{a_2} \phi'(0, y') \cos(k_m y') dy' \]  
\[ (A3) \]

\[ C_d^i = \frac{2}{(\alpha_2 - \alpha_1)} \int_{a_i}^{a_2} \phi'(L, y') \cos(k_m y') dy' \]  
\[ (A4) \]

\[ \alpha_1(m) = \frac{2L}{m\pi} \left[ \frac{1 - \cos(k_m x_p) V_{eff}(0)}{2 \cosh(k_m t_{ax})} \right. \] 
\[ \left. \cos(k_m x_p) - (-1)^m V_{eff}(L) \right] + \sum_n \left( C_s^i + (-1)^{m+1} C_d^i \right) \frac{k_m}{k_n^2 + k_m^2} \]  
\[ (A5) \]

\[ \alpha_2(m) = \frac{2L}{m\pi} \left[ \int_0^{L_{poly}} \frac{\rho(x', y')}{\varepsilon_{Si}} G(x, y; x', y') dx' \right] \left[ \int_0^{L_{poly}} \sin(k_m x) dx \right] + C_s^i \left( \frac{1 - (-1)^m}{k_m} \right) + C_d^i \left( \frac{(-1)^{m+1}}{k_m} \right) + \sum_n \left( C_s^i + (-1)^{m+1} C_d^i \right) \frac{k_m}{k_n^2 + k_m^2} \]  
\[ \left( \frac{L_{poly}}{y'_{poly}} \right) \]  
\[ (A6) \]

\[ \beta_1(m) = \left[ \frac{1 - (-1)^m}{k_m} \right] + C_s^i \left( \frac{(-1)^{m+1}}{k_m} \right) + \sum_n \left( C_s^i + (-1)^{m+1} C_d^i \right) \frac{k_m}{k_n^2 + k_m^2} \]  
\[ (A7) \]

\[ \beta_2(m) = \sum_n \left( C_s^i + (-1)^{m+1} C_d^i \right) \frac{k_m}{k_n^2 + k_m^2} \]  
\[ (A8) \]

\[ \gamma_1 = \frac{1}{2m\pi} \left( \frac{\text{tanh}(k_m t_{ax})}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{Si} \text{tanh}(k_m t_{poly})} \right) \]  
\[ (A9) \]

\[ \gamma_2 = \frac{1}{2m\pi \varepsilon_{Si} \text{sinh}(k_m t_{poly})} \]  
\[ (A10) \]

\[ \gamma_3 = \frac{1}{2m\pi} \left( \frac{\text{tanh}(k_m t_{ax})}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{Si} \text{tanh}(k_m t_{poly})} \right) \]  
\[ (A11) \]

\[ D^e_m = \frac{(\alpha_1 - \alpha_2) \gamma_3 - (\beta_2 - \beta_1) \gamma_2}{\gamma_1 \gamma_3 - \gamma_1^2} \]  
\[ (A12) \]

\[ D^b_m = \frac{(\alpha_1 - \alpha_2) \gamma_2 - (\beta_2 - \beta_1) \gamma_1}{\gamma_1 \gamma_3 - \gamma_2^2} \]  
\[ (A13) \]

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